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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PING-SHENG TSENG, SHARON SHEAU-PYNG LIN, QUINCY KUN-HSU SHEN, MIKE MON YEN TSAI and STEVEN WANG

Appeal 2009-004277
Application 09/954,715
Technology Center 2100

Before HOWARD B. BLANKENSHIP, JEAN R. HOMERE, and CAROLYN D. THOMAS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-50. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

According to Appellants, the invention relates to "electronic design automation (EDA)" (Spec. 1:13). In particular, the present invention involves "dynamically changing the evaluation period to accelerate design debug sessions" (Spec. 1:14-15).

Claim 1 is illustrative:

1. An electronic design automation system for verifying a user design, comprising:

a computing system including a central processing unit for modeling the user design in software;

an internal bus system coupled to the computing system;

reconfigurable hardware logic coupled to the internal bus system and for generating a hardware model which includes at least a portion of the user design modeled in hardware;

control logic coupled to the internal bus system for controlling the delivery of data between the reconfigurable hardware logic and the computing system; and

shared memory for holding a first information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the hardware model and the software model is capable of directly accessing the second information of the hardware model.

Rejections

R1: Claims 1-6, 19-36, 38, and 44-46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhandari et al. (U.S. Patent No. 5,663,900, Sep. 2, 1997) and Klein (U.S. Patent No. 5,771,370, Jun. 23, 1998).

R2: Claims 7 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhandari, Klein, and in further view of Fred U. Rosenberger, *Q-Modules: Internally Clocked Delay-Insensitive Modules*, 37 IEEE Transactions on Computers 1005 (Sep. 1998) ("Rosenberger").

R3: Claims 8, 9, and 11-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhandari, Klein, Rosenberger and W.S. VanSheik *High Speed External Asynchronous/Internally Clocked Systems,* 46 IEEE Transactions on Computers 824 (Jul. 1997) ("VanScheik").

R4: Claim 37 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhandari, Klein and Butts (U.S. Patent No. 5,661,662, Aug. 26, 1997).

R5: Claims 39-43 and 47-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bhandari, Klein, and William D. Bishop, *A Heterogeneous Environment for Hardware/Software Cosimulation,* IEEE Transactions on Computers, 14 (1997) ("Bishop").

GROUPING OF CLAIMS

Appellants argue claims 1-6, 19-36, 38, and 44-46 as a group (App. Br. 10-16). Appellants argue claims 7-18, 37, 39-43, and 47-50 based on arguments made with respect to claim 1, and do not present separate arguments for patentability of claims 7-18, 37, 39-43, and 47-50 (*see* App. 16-19). We select independent claim 1 as the representative claim. We will, therefore, treat claims 2-50 as standing or falling with representative claim 1.

FINDINGS OF FACT (FF)

Bhandari Reference

1. Bhandari discloses:

> Interface software and hardware is provided between the simulated prototype definition 32 and external systems 44, 46 to provide distributed or multiple access paths for cooperative processing and signal processing therebetween. In this manner, specified signal paths or interconnection lines are provided, as specified by a design engineer, from CAE tool 14 to particular sockets pins or electrical contacts or nodes in particular external systems 44, 46 from particular simulator 16. (col. 3, ll. 21-29).

Pauna Reference

2. Pauna discloses:

> Co-verification simulators known in [the] art typically determine the internal behavior and state of hardware and software components every cycle of a simulator…. Cycle-accurate simulator 12 in a preferred embodiment of the present invention allows events to be set and the internal behavior and state of hardware components to be accurately examined at specific events (e.g., after a memory access) …. Cycle-accurate simulate 12 can also determine internal behavior and state of

hardware and software components every cycle by setting a first event to occur on a first simulator cycle and a second event to occur on a second simulator cycle .... (col. 14, ll. 22-36).

Klein Reference

3. Klein discloses:

[A] hardware-software system co-simulation 10 comprising hardware and software simulations 12 and 18, is performed with a single coherent view 22 of the memory of the hardware-software system being co-simulated. . . . Preferably, this single coherent view 22 may further include a memory segment 34 being viewed as having been configured for software simulation access only, a memory segment 38 being viewed as having been configured for hardware simulation access only ....

(Col. 4, ll. 16-42; *see also* FIG. 1).

PRINCIPLES OF LAW

Obviousness

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine,* 837 F.2d 1071, 1073 (Fed. Cir. 1988). If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker,* 977 F.2d 1443, 1445 (Fed. Cir. 1992).

ANALYSIS

Claims 1-50

Issue 1a: Did the Examiner err in finding that the combination of cited references, particularly Klein, discloses a "shared memory for holding a first information of a software model and a second information of the hardware model," as set forth in claim 1?

Appellants argue that "[i]n contrast to Appellants' invention, the 'single coherent view of memory' in Klein is an abstract or logical construct of a memory portion of the hardware-software design being simulated," and it is not a tangible or physical memory (*see* App. Br. 14-15).

The Examiner finds that the "claim does not recite a physical shared memory and … does not differentiate between the logical and physical memory as argued (Ans. 29). The Examiner further found that "Klein teaches shared (coherent) memory for holding first information of software model, and second information of the hardware model." (Ans. 6.) We agree.

We find that Appellants are merely arguing limitations that are not claimed. Claim 1 recites, *inter alia*, a "shared memory for holding a first information…" (App. Br. 21, Claims App'x). The claimed "shared memory" is not limited to any particular type of memory, i.e., physical memory. We remind Appellants that the *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). Furthermore, "limitations are not to be read into the claims from the specification." *In re Van Geuns,* 988 F.2d 1181, 1184 (Fed. Cir. 1993)

(citing *In re Zletz,* 893 F.2d 319, 321 (Fed. Cir. 1989)). Here, Appellants by their arguments are attempting to read the phrase "shared *physical* memory" into claim 1. However, claim 1 is written more broadly than argued. As such, we find that all that is required in claim 1 is a "shared memory" that holds the claimed features, i.e., first information of a software model and second information of the hardware model.

Klein discloses a single coherent view of a memory that includes both a software simulation segment and a hardware simulation segment (FF 3). In other words, Klein's memory holds "information" relating to software and hardware simulation of the system.

In any case, the *type* of information being held by the shared memory is non-functional descriptive material, which should not be given any patentable weight. In a precedential decision, an expanded panel recently held that elements that do not affect the claimed process are nonfunctional material and are merely descriptive. *See Ex parte Nehls*, 88 USPQ2d 1883, 1887-88 (BPAI 2008) (precedential) *available at* http://www.uspto.gov/web/offices/ dcom/bpai/prec/fd071823.pdf.[2] We note that functional descriptive material consists of data structures or computer programs which impart functionality when employed as a computer component. In contrast, nonfunctional descriptive material refers to data content that does not exhibit a functional interrelationship with the substrate and does not affect the way the computing processes are performed. *See* MPEP § 2106.01 ("'Nonfunctional descriptive material' includes but is not limited to music, literary works, and a compilation or mere arrangement of

[2] *See also Ex parte Mathias*, 84 USPQ2d 1276 (BPAI 2005) (informative) (*aff'd* 191 Fed. Appx. 959 (Fed. Cir. 2006)).

data.").

Nonetheless, as noted *supra,* we find that Klein discloses a shared memory for holding a first information of a software model and a second information of the hardware model. Accordingly, we find that Appellants have failed to persuade us that the Examiner erred in finding that Klein teaches a "shared memory for holding a first information of a software model and a second information of the hardware model," as set forth in claim 1.

Issue 1b: Did the Examiner err in finding that the combination of references, particularly Bhandari, discloses "second information comprises at least one internal state of the hardware model," as set forth in claim 1?

Appellants contend that "'determining' internal behavior and state of hardware and software components does not teach or suggest storing them in a shared memory." (App. Br. 11.)

The Examiner cites col. 3, lines 21-29 of Bhandari, and finds that "BH '900 teaches that the second information comprises at least one internal state of the hardware model, and "takes official notice that … such information would be vital to [] any hardware-software co-simulation system" (Ans. 5) (emphasis omitted).

The Examiner has shown that Bhandari discloses cooperative processing between the software and hardware simulated prototype systems (FF 1). As such, the Examiner reasoned that that software model is capable of directly accessing the second information. We agree. Furthermore, Appellants have not shown that such a system is incapable of performing this function. The Examiner further takes official notice that it is known in

simulation environments to have information concerning the internal state of the hardware model, and the Examiner imports an additional reference, Pauna, to show this fact.

For instance, Pauna teaches that "[c]o-verification simulators known in [the] art typically determine the internal behavior and state of hardware components (e.g., after a memory access)" (FF 2). We find that both Bhandari and Klein relate to co-verification simulation environments. Accordingly, Pauna supports the Examiner's reasonable official notice that the combination of cited references teach that "the second information comprises at least one internal state of the hardware model," as set forth in claim 1.

DECISION

The Examiner's rejection of claims 1-50 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2010).

AFFIRMED

APJ INITIALS:

ke

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Application 09/954,715

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